



Books & Reports

Parallel Subconvolution Filtering Architectures

These architectures are based on methods of vector processing and the discrete-Fourier-transform/inverse-discrete-Fourier-transform (DFT-IDFT) overlap-and-save method, combined with time-block separation of digital filters into frequency-domain subfilters implemented by use of sub-convolutions. The parallel-processing method implemented in these architectures enables the use of relatively small DFT-IDFT pairs, while filter tap lengths are theoretically unlimited. The size of a DFT-IDFT pair is determined by the desired reduction in processing rate,

rather than on the order of the filter that one seeks to implement. A report presents additional information on the parallel, discrete-time, sub-convolution filtering architectures that lie at the heart of the innovation described in "Modular, Parallel, Efficient Pulse-Shaping Filters" (NPO-30186) elsewhere in this issue of NASA Tech Briefs. The emphasis in the report is on those aspects of the underlying theory and design rules that promote computational efficiency, parallel processing at reduced data rates, and simplification of the designs of very-large-scale integrated (VLSI) circuits needed to implement high-order filters and correlators.

This work was done by Andrew A. Gray of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to

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Refer to NPO-30142, volume and number of this NASA Tech Briefs issue, and the page number.